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| 09/892,291 | 06/25/2001 | Joseph Weiyeh Ku | 10008039-1 | 2125 |

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| EXAMINER | |
|---|---|
| MANOSKEY, JOSEPH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2113 | |

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/892,291 | KU, JOSEPH WEIYEH | |
| | Examiner | Art Unit | |
| | Joseph Manoskey | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 11 recites the limitation "The data structure" in line 1. There is insufficient antecedent basis for this limitation in the claim. This claim is dependent upon claim 3, it is believed that this claim should dependent upon claim 10. For the purposes of further examination claim 11 is interpreted as being dependent upon claim 10.

### *Claim Rejections - 35 USC § 101*

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 10 and 11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed subject matter is a data structure per se and is non-statutory subject matter.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 5, 6, 13, 14, 16, 17, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shephard, III et al., U.S. Patent 5,633,877, hereinafter referred to as "Shephard".

8. Referring to claim 1, Shephard discloses a method for chip testing that includes establishing a link between a chip and a tester, Shephard describes scanning in instructions to the BIST, this is interpreted as a link between a chip and a tester (See Col. 1, lines 64-67). Shephard teaches the instructions scanned in being logical test

vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out over the communications link (See Col. 2, lines 48-53).

9. Referring to claim 2, Shephard teaches the method including scanning in subsequent test scenarios (See Col. 2, line 53).

10. Referring to claim 3, Shephard discloses the testing being of a memory array of the chip (See Col. 1, lines 50-52).

11. Referring to claim 5, Shephard teaches the results of the test being the failed address (See Col. 3, lines 18-20).

12. Referring to claim 6, Shephard discloses the testing including writing the data into the array, reading it out of the array, comparing the data read out with the expected data, and providing the address of the failed addresses (See Col. 3, lines 13-20).

13. Referring to claim 13, Shephard discloses a programmable BIST for chip testing that includes establishing a link between a chip and a tester, Shephard describes scanning in instructions to the BIST, this is interpreted as a link between a chip and a tester (See Col. 1, lines 49-50 and 64-67). Shephard teaches the instructions scanned

in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out over the communications link (See Col. 2, lines 48-53).

14. Referring to claim 14, Shephard discloses the testing being of a memory array of the chip (See Col. 1, lines 50-52).

15. Referring to claim 16, Shephard teaches the results of the test being the failed address (See Col. 3, lines 18-20).

16. Referring to claim 17, Shephard discloses the testing including writing the data into the array, reading it out of the array, comparing the data read out with the expected data, and providing the address of the failed addresses (See Col. 3, lines 13-20).

17. Referring to claim 20, Shephard discloses a system for chip testing that includes establishing a link between a chip and a tester, Shephard describes scanning in instructions to the BIST, this is interpreted as a link between a chip and a tester (See Fig. 2 and 3, and Col. 1, lines 64-67). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the

algorithm, gathering the results and scanning them out over the communications link (See Col. 2, lines 48-53).

18. Referring to claim 21, Shephard discloses a system for chip testing that includes establishing a link between a chip and a tester, Shephard describes scanning in instructions to the BIST, this is interpreted as a link between a chip and a tester (See Fig. 2 and 3, and Col. 1, lines 64-67). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses the testing being of a memory array of the chip (See Fig. 2 and Col. 1, lines 50-52). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out over the communications link (See Col. 2, lines 48-53).

19. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Bhavsar et al., U.S. Patent 6,408,401, hereinafter will be referred to as "Bhavsar".

20. Referring to claim 10, Bhavsar discloses a fault bitmap that is off-loaded to the test system (See Col. 4, lines 31-32). This fault bitmap is interpreted as a data structure containing failed memory information of the on-chip BIST and sent over a communication link. The bitmap includes row address fields and column address fields. Together these fields are interpreted as a failed address field. In addition to not only

providing the failed address they also provide the failed cell location in the array, which is interpreted as the bailed bit location (See Col. 2, line 60 to Col. 3, line 6).

***Claim Rejections - 35 USC § 103***

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 4, 7, 8, 12, 15, 18, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shephard in view of Bhavsar.

23. Referring to claim 4, Shephard teaches all the limitations (See rejection of claim 3) except for the generating a bit-map from the failure information of failed bit locations within the memory array, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the testing method of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the invention to

do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

24. Referring to claim 7, Shephard discloses all the limitations (See rejection of claim 6) except for adding failed bit locations of the failed address, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory, it is interpreted that the bit-map contains the failed bits of the failed memory location (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the testing method of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

25. Referring to claim 8, Shephard discloses all the limitations (See rejection of claim 1) except for repairing the chip using redundancy allocation techniques based on the set of failure information. Bhavsar teaches using spare rows and/or columns to replace failed ones (See Col. 2, lines 22-29). Bhavsar also teaches the repair solution being based on extracted failure information from the test (See Col. 4, lines 64-65). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the repair scheme with redundancy of Bhavsar with the chip testing method of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the

invention to do this because the scheme of Bhavsar provides a higher yield of chips during manufacture (See Col. 2, lines 2-5).

26. Referring to claim 12, Shephard discloses a method for chip testing that includes establishing a link between a chip and a tester, Shephard describes scanning in instructions to the BIST, this is interpreted as a link between a chip and a tester (See Col. 1, lines 64-67). Shephard discloses the testing being of a memory array of the chip (See Col. 1, lines 50-52). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out over the communications link (See Col. 2, lines 48-53). Shephard also discloses the testing including writing the data into the array, reading it out of the array, comparing the data read out with the expected data, and providing the address of the failed addresses (See Col. 3, lines 13-20). Shephard does not teach the generating a bit-map from the failure information of failed bit locations within the memory array or adding failed bit locations of the failed address, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory, it is interpreted that the bit-map contains the failed bits of the failed memory location (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar

with the testing method of Shephard. This would have been obvious to do because it allows for a repair solution to be determined (See Col. 1, lines 48-49).

27. Referring to claim 15, Shephard teaches all the limitations (See rejection of claim 14) except for the generating a bit-map from the failure information of failed bit locations within the memory array, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the medium of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

28. Referring to claim 18, Shephard discloses all the limitations (See rejection of claim 17) except for adding failed bit locations of the failed address, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory, it is interpreted that the bit-map contains the failed bits of the failed memory location (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the medium of Shephard. This would have been obvious to one of ordinary skill in the

art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

29. Referring to claim 19, Shephard discloses all the limitations (See rejection of claim 13) except for repairing the chip using redundancy allocation techniques based on the set of failure information. Bhavsar teaches using spare rows and/or columns to replace failed ones (See Col. 2, lines 22-29). Bhavsar also teaches the repair solution being based on extracted failure information from the test (See Col. 4, lines 64-65). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the repair scheme with redundancy of Bhavsar with the medium of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because the scheme of Bhavsar provides a higher yield of chips during manufacture (See Col. 2, lines 2-5).

30. Referring to claim 22, Shephard discloses all the limitations (See rejection of claim 21) except for repairing the chip using redundancy allocation techniques based on the set of failure information. Bhavsar teaches using spare rows and/or columns to replace failed ones (See Col. 2, lines 22-29). Bhavsar also teaches the repair solution being based on extracted failure information from the test (See Col. 4, lines 64-65). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the repair scheme with redundancy of Bhavsar with the system of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the

invention to do this because the scheme of Bhavsar provides a higher yield of chips during manufacture (See Col. 2, lines 2-5).

31. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shephard in view of Bosse, U.S. Patent 4,586,178.

32. Referring to claim 9, Shephard teaches all the limitations (See rejection of claim 1) except for identifying a number of circuit redundancies within the chip and halting the testing if the failure information exceeds the number of redundancies. Bosse discloses aborting a test if assigning a redundant row or column to repair a faulty original one is not possible because the supply of redundant rows or columns has been exhausted (See Col. 8, lines 44-52). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the redundant memory and aborting a test of Bosse with the chip testing method of Shephard. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it alerts the user to the fact that it is not possible to repair the memory (See Bosse, Col. 9, lines 3-6).

33. Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhavsar in view of Orita et al., U.S. Patent 6,499,119, hereinafter referred to as "Orita".

34. Referring to claim 11, Bhavsar discloses all the limitations (See rejection of claim 10) including Bhavsar teaches the having both the data written in to the memory and the

data read out of the memory (See Col. 2, lines 10-12). Bhavsar does not teach the data structure having a header field and length fields. Orita discloses a delimiter at the beginning of a data structure, this is interpreted as a header. Orita also teaches the use of a length field. Orita teaches the data structure including the pattern data (See Fig. 1). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the data structure of Orita with the data structure of Bhavsar. This would have been obvious to one of ordinary skill in the art at the time of the invention because it allows a way to specify the location of where a fault is generated (See Orita, Col. 1, line 66 to Col. 2, line 3).

***Conclusion***

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are prior art that of memory with BIST that is closely related.

U.S. Patent 6,400,173 to Shimizu et al.

U.S. Patent 6,643,807 to Heaslip et al.

U.S. Patent 5,912,901 to Adams et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
February 27, 2004

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